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Study of a harmonic current compensation system using a hysteresis-controlled active filter: Design, sizing and optimization

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Abstract

This article presents a comprehensive study on the design, sizing, and optimization of a parallel active filter (FAT1) using a hysteresis control strategy for harmonic current compensation in an industrial environment. The study, conducted at the BRALIMA/Kinshasa industrial complex, is based on experimental measurements revealing a THDi of 43.95% with a dominance of harmonics of rank 5 (38%) and 7 (16%). The article details the analytical sizing methodology, rigorous parametric calculations, and technical compromises necessary for the industrial implementation of the system.

Keywords: Active Filter; Hysteresis Control; Harmonic Currents; Analytical Sizing; Power Quality; Three-Phase Inverter; Active Compensation

1. Introduction

The deterioration of the quality of electrical energy due to harmonic currents represents a major challenge for modern industrial installations. Variable speed drives, although optimizing energy efficiency, generate significant harmonics that alter equipment performance and increase losses. This article presents the development of the Tanganyi Series 1 Active Filter (FAT1), specifically designed to mitigate these disturbances in the Congolese industrial context [2, 5].

2. Architecture and sizing of the FAT1

2.1. General design

The FAT1 is based on a three-phase voltage inverter requiring three fundamental elements: a reference voltage, an energy storage system, and an output filter [3]. These components are controlled by a sophisticated control circuit that allows for the identification and injection of harmonic currents in opposite phase.

2.2. Sizing of the DC bus voltage

The theoretical reference voltage is calculated according to the equation:

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$$V_{0ref} = 2(V_m + L_r\omega_1 I_{ond}) \qquad \text{eq. (1)}$$

With:

$V_m = 230\sqrt{2} = 325{,}27\ \text{V}$ (voltage amplitude)

$L_r = 0{,}16\ \mu\text{H}$ (line inductance)

$$\omega_1 = 2\pi \times 50 = 314{,}16\ \text{rad/s}$$

$I_{ond} = I_5 = 10{,}18\ \text{A}$ (dominant harmonic current)

The calculation gives $V_{0ref} = 650{,}54\ \text{V}$. An operational voltage of $V_0 = 600\ \text{V}$ is retained, offering a margin of 50.54 V for control dynamics while meeting the condition $V_0 > \sqrt{3} \times V_m = 563{,}38\ \text{V}$ to avoid overmodulation.

2.3. Sizing of the storage capacitor

Two analytical methods are applied:

2.3.1. Method 1 (based on dominat harmonics)

$$C = \frac{V_r\sqrt{I_5^2+I_7^2}}{2\omega\varepsilon V_0^2} = 224{,}6\ \mu\text{F} \qquad \text{eq. (2)}$$

2.3.2. Method 2 (based on the lowest frequency harmonic)

$$C = \frac{I_3}{\varepsilon V_0 \omega_3} = 27{,}6\ \mu\text{F} \qquad \text{eq. (3)}$$

A compromise leads to the selection of a standardized capacitor of C=100 µF, balancing response speed and stability.

2.4. Characterization of losses

The active power required to compensate for internal losses is:

$$P_{pertes} = \frac{V_0^2}{R} = \frac{600^2}{52{,}5} = 6{,}86\ \text{kW} \qquad \text{eq. (4)}$$

With a corresponding current of $I_{losses} = 11{,}43\ \text{A}$.

2.5. Switching tables and vector representation

Table 1 presents the 8 switching states of the 600V three-phase inverter, while Table 2 shows their transformation in the αβ (Concordia) plane [6].

Table 1 Switching states of the three-phase inverter (V_0 = 600 V)

Etat	u_1	u_2	u_3	V_{f1}	V_{f2}	V_{f3}	$V_{f1} - V_{f2}$	$V_{f2} - V_{f3}$	$V_{f3} - V_{f1}$
1	0	0	0	0	0	0	0	0	0
2	0	0	1	-200	-200	400	0	-600	600
3	0	1	0	-200	400	-200	-600	600	0
4	0	1	1	-400	200	200	-600	0	600
5	1	0	0	400	-200	-200	600	0	-600
6	1	0	1	200	-400	200	600	-600	0
7	1	1	0	200	200	-400	0	600	-600
8	1	1	1	0	0	0	0	0	0

Table 2 Voltage vectors in the αβ plane

Etat	V_α	V_β	Module	Angle
1	0	0	0	-
2	0	$-\sqrt{(2/3)} \times 600$	489.9	270°
3	$\sqrt{(2/3)}\times300$	$\sqrt{(2/3)}\times300$	489.9	60°
4	$\sqrt{(2/3)}\times300$	$-\sqrt{(2/3)}\times300$	489.9	0°
5	$-\sqrt{(2/3)}\times300$	$-\sqrt{(2/3)}\times300$	489.9	180°
6	$-\sqrt{(2/3)}\times300$	$\sqrt{(2/3)}\times300$	489.9	120°
7	0	$\sqrt{(2/3)}\times600$	489.9	60°
8	0	0	0	-

These vectors, of constant amplitude (489.9 V), allow for the synthesis of any voltage within the hexagon of the αβ space via the SVPWM technique.

3. Hysteresis control strategy

3.1. Principle and configuration

Hysteresis control keeps the compensation current within a band ΔI around the reference. The sizing of this band constitutes a critical compromise between accuracy and switching frequency.

3.2. Sizing of the hysteresis band

3.2.1. The theoretical relationship

$$\Delta I = \frac{V_0 \cdot T_{min}}{L_f} \qquad \text{eq. (5)}$$

with $T_{min} = 1/f_{max}$ et $f_{max} = 20$ kHz, initially leads to $\Delta I = 187\,500$ A for $L_f = 0{,}16$ μH. A pragmatic approach based on the measured harmonic current ($I_H = 11{,}427$ A) donne $\Delta I = 2{,}0$ A (17,5% de I_H).

3.3. Adjustment of the coupling inductance

3.3.1. The estimated switching frequency

$$f_{comm} = \frac{V_0}{4 \cdot L_f \cdot \Delta I} \qquad \text{eq. (6)}$$

initially reaches 468.75 kHz. Adjusting L_f à 1,0 mH reduces this frequency to a theoretical 75 kHz, with a practical value of approximately 15 kHz.

3.4. PI controller synthesis

The DC voltage regulation system is modeled by:

$$F(s) = \frac{K}{1+\tau s} = \frac{25\,615}{1+0{,}000756s} \qquad \text{eq. (7)}$$

The gains of the PI regulator are calculated with $\tau_d = 0{,}02$ s:

$$K_p = 1{,}476 \times 10^{-6}, K_i = 1{,}952 \times 10^{-3}$$

3.5. Sizing of the output filter

The output inductance is sized to ensure sufficient dynamics up to the 50th harmonic. [4]:

$$L_f \leq \frac{V_0}{\omega_{max} \cdot \Delta I_{max}} = 16{,}7\ \text{mH} \qquad \text{eq. (8)}$$

with $\omega_{max} = 2\pi \times 2500 = 15\,708$ rad/s et $\Delta I_{max} = 2{,}285$ A (20% de I_H).

3.6. Synthesis of parameters

Table 3 Complete parameters of the FAT1 system

Category	Parameter	Value	Unit
Network	Nominal voltage	230	V
	Frequency	50	Hz
Measured harmonics	Initial THDi	43,95	%
	I_5 (5th order)	10,18	A
	I_7 (7th order)	4,29	A
FAT1 - Power circuit	DC bus voltage	600	V
	Capacity	100	µF
	Equivalent resistance	52,5	Ω
	Internal losses	6,86	kW
FAT1 - Hysteresis control	Coupling inductance	1,0	mH
	Hysteresis band	2,0	A
	Switching frequency	≈15	kHz
Regulation	K_p	$1{,}476\times10^{-6}$	-
	K_i	$1{,}952\times10^{-3}$	s^{-1}

3.7. Performances and validation

3.7.1. Compensation results

- THDi reduction: 43.95% → 5.8% (86.8% improvement)
- Improvement of the power factor: 0.830 → 0.906 (+9.2%)
- Reduction of distorting power: 10.72 → 1.27 kVAr (-88.2%)

3.7.2. Critical energy balance

- Line losses saved: 51.3 W
- FAT1's own losses: 190.6 W
- Net balance: -139.3 W (unfavorable)
- Energy Return Ratio (ERR): 0.27 (not energetically profitable)

4. Conclusion

The study demonstrates the technical effectiveness of FAT1 for harmonic compensation, with performance compliant with IEC standards. However, the unfavorable energy balance highlights the necessary trade-off between power quality and energy efficiency in active filtering applications. The sized and optimized parameters provide a solid foundation for industrial implementation, with prospects for improvement thru the integration of advanced modulation techniques and the optimization of passive components.

Compliance with ethical standards

Disclosure of conflict of interest

No conflict of interest to be disclosed.

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